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EXAMINER
WARREN, MATTHEW E

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ANDREW MARSHALL

Appeal 2007-2712
Application 10/007,332
Technology Center 2800

Decided: February 7, 2008

Before JOSEPH F. RUGGIERO, ANITA PELLMAN GROSS, and MARC S. HOFF, *Administrative Patent Judges*.

GROSS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Marshall (Appellant) appeals under 35 U.S.C. § 134 from the Examiner's Final Rejection of claims 6 through 13 and 15 through 19, which are all of the claims pending in this application. We have jurisdiction under 35 U.S.C. § 6(b).

Appellant's invention relates generally to a silicon-on-insulator (SOI) integrated circuit structure in an analog application. *See* Spec. 1-3. Claim 6 is illustrative of the claimed invention, and it reads as follows:

6. An integrated circuit semiconductor-on-insulator circuit structure, comprising:

a pair of transistors in an analog circuit stage which requires matched behavior of said pair;

a physical connection of metallic material which provides thermal conduction between respective bodies of said pairs of transistors; and

an insulating layer beneath said pair;

an insulating barrier substantially surrounding said pair and extending to said insulating layer.

The prior art references of record relied upon by the Examiner in rejecting the appealed claims are:

Houston	US 6,037,808	Mar. 14, 2000
Flaker	US 6,133,608	Oct. 17, 2000

Claims 10 through 13 and 15 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement.

Claims 6, 9, and 16 through 19 stand rejected under 35 U.S.C. § 102(a)[1] as being anticipated by Flaker.

Claims 10 through 13 and 15 stand rejected under 35 U.S.C. § 102(a)[2] as being anticipated by Houston.

Claims 7 and 8 stand rejected under 35 U.S.C. § 103 as being unpatentable over Flaker in view of Houston.

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[1] We note that the Examiner has applied 35 U.S.C. § 102(a) although he should have used 35 U.S.C. § 102(e), since the reference is a US patent with a filing date prior to the filing date of the application. However, we consider this a harmless error.

[2] Again the Examiner has applied 35 U.S.C. § 102(a) instead of §102(e).

We refer to the Examiner's Answer (mailed May 23, 2006) and to Appellant's Brief (filed January 18, 2006) for the respective arguments.

SUMMARY OF DECISION

As a consequence of our review, we will affirm the first paragraph and anticipation rejections of claims 10 through 13 and 15 and also the anticipation rejection of claims 16 through 19, but we will reverse the anticipation rejection of claims 6 and 9 and the obviousness rejection of claims 7 and 8.

OPINION

The Examiner asserts (Ans. 4) that the language "wherein said bodies are not tied to any fixed potential through a low impedance path," added by amendment to claim 10, is not enabled by the originally filed Specification. The Examiner explains (Ans. 9) that the Specification supports the bodies not being tied to a fixed potential. However, "limiting that tie to a low impedance path suggests that other impedance types may be used," and the Specification makes no mention of an impedance path. Appellant contends (Br. 7-8) that statements in the Specification that the transistor body is left floating and that the structures have electrical isolation from external sources provide support for the claim language at issue. However, the portions of the Specification relied upon by Appellant merely indicate that the bodies are not tied to any fixed potential. Appellant has not indicated what portion of the Specification supports the entire limitation, "said bodies are not tied to any fixed potential *through a low impedance path*" (emphasis added).

Therefore, we will sustain the rejection of claims 10 through 13 and 15 under 35 U.S.C. § 112, first paragraph.

With regard to the anticipation rejection of claims 6 and 9 over Flaker, Appellant contends (Br. 8) that although metals have properties of electrical and thermal conduction, Flaker's metal connection between respective bodies of the transistors does not necessarily provide "good thermal properties." Further, Appellant contends (Br. 9) that the metal connection taught by Flaker is only disclosed for digital applications. Last, Appellant contends (Br. 9) that Flaker adds an extra oxide layer which "would reduce the thermal coupling," which therefore "teaches away from providing thermal conduction."

The Examiner asserts (Ans. 10) that Appellant admits that Flaker's metal has the property of thermal conduction, just not "good" thermal conduction. Further, even if the extra oxide layer reduces thermal coupling, there is still some thermal conduction. (*See* Ans. 11.) According to the Examiner (Ans. 10), since "the claims do not place limits on the amount of thermal conduction," the provision of thermal conduction is satisfied by Flaker. The Examiner additionally asserts (Ans. 10) that Flaker does not require a digital application for the metal link to be formed of metal.

Thus, the issues before us for claims 6 and 9 are whether Flaker's metal connection between respective bodies of the transistors a) provides thermal conduction and b) is disclosed as being applicable to analog applications, as recited in the claims.

As to whether the metal connection provides thermal conduction, we agree with the Examiner that it does. As pointed out by the Examiner, the claims do not quantify the amount or specify the quality of thermal

conduction provided, but merely require that some thermal conduction is provided. Appellant admits that metals have thermal properties (Br. 8) and that the metal provides thermal conduction (Br. 9) or the referenced oxide layer could not "reduce" the thermal conduction.

However, regarding whether Flaker uses a metal connection in analog applications, we disagree with the Examiner. Flaker explicitly states (col. 6, l. 66-col. 7, l. 4), "while the invention has been shown and described as using silicon for the conductive material of the selective link, it is to be understood that such conductive material may include any suitable conductive material such as metal, …, *as appropriate and/or suitable for a particular SOI memory circuit application*" (emphasis added). Thus, Flaker clearly discloses metal for memory circuits, but does not indicate that metal would also be good for analog applications. Accordingly, we cannot sustain the anticipation rejection of claims 6 and 9 over Flaker.

For the anticipation rejection of claim 16 over Flaker, Appellant (Br. 10-12) presents substantially the same arguments as for the rejection of claim 6. Specifically, Appellant contends that metals don't necessarily have "good thermal properties" and the addition of an extra oxide layer would "reduce" thermal coupling and, thus, teach away from providing thermal conduction. Also, Appellant contends that Flaker teaches "equilibration of the body charge differentials due to thermal effects … which is entirely different than equalizing the thermal effects."

Like claim 6, independent claim 16 does not require "good" thermal conduction, just some thermal conduction. Further, by arguing that Flaker's oxide layer will "reduce" the thermal coupling, Appellant is admitting that there is some thermal conduction. In addition, as claim 16 does not recite

equalizing thermal effects, Appellant's argument is not commensurate in scope with the claim. Therefore, we will sustain the anticipation rejection of claim 16. We will also sustain the anticipation rejection of claim 17, since Appellant (Br. 12) has merely restated the limitation, which is not considered an argument in accordance with our rules, and which fails to respond to the specifics of the rejection set forth by the Examiner.

With regard to claim 18, Appellant contends (Br. 13) that Flaker "does not provide an enabling description of the use of Flaker's circuit in an analog circuit stage." The Examiner (Ans. 6) points out that Flaker discloses that the transistors can be used in circuits such as a differential amplifier, which is a type of analog circuit. Therefore, the use of Flaker's circuit in an analog circuit stage is disclosed. As to the description of said use being enabling, Flaker's disclosure is no less enabling than Appellant's disclosure. Accordingly, we will sustain the anticipation rejection of claim 18 over Flaker.

Claim 19 recites that the "physical connection does not carry current during normal operation of said circuit stage." The Examiner (Ans. 6) explains why Flaker's intrinsic silicon connection will not conduct electricity during normal operation. Appellant contends (Br. 13) that Flaker's silicon connection "will still conduct electricity (though it may indeed be a poor conductor compared to highly doped silicon)." Since Appellant uses as a preferred embodiment a p-doped semiconductor connection, it is unclear how Appellant's connection will conduct electricity less than Flaker's semiconductor connection. Accordingly, to the extent that Appellant's connection does not carry current during normal operation of the circuit stage, we find that Flaker's silicon connection does not carry current during

normal operation. Thus, we will sustain the anticipation rejection of claim 19.

Regarding independent claim 10, Appellant contends (Br. 14) that Houston does not disclose a physical connection providing thermal conduction. Appellant contends (Br. 14) that "configurations having good electrical conduction don't necessarily have good thermal properties." The Examiner (Ans. 11) replies that Houston's materials and structure are the same as Appellant's, and, therefore, Houston's connection inherently provides thermal conduction. The issue is whether Houston's physical connection of the transistor bodies provides thermal conduction.

We agree with the Examiner. Houston's connection is made of a P-type semiconductor, just as Appellant's. (*See* Houston, col. 9, ll. 35-40, and Appellant's Specification 3:4-5, 9:12-14.) Appellant has not explained why or how Houston's connection fails to provide thermal conduction whereas Appellant's does thermally conduct. Thus, we find that Houston's connection thermally conducts to the same extent Appellant's connection does. Since Appellant has presented no further arguments, we will sustain the anticipation rejection of claim 10 over Houston. We will also sustain the anticipation rejection of claims 11 through 13 and 15, since Appellant merely restates the additional limitations, which is not considered an argument in accordance with our rules, and which fails to respond to the specifics of the Examiner's rejection.

The Examiner rejects claims 7 and 8 under 35 U.S.C. § 103 as being unpatentable over Flaker in view of Houston. Appellant contends (Br. 16-17) that Houston fails to cure the deficiency of Flaker. We agree. As indicated *supra*, Flaker fails to disclose a metal connection in an analog

circuit stage. Houston discloses (col. 9, ll. 35-40) connecting the transistor bodies with a P-type semiconductor region. Since Houston does not disclose using metal for the connection, Houston cannot provide a reason to substitute metal for the connection in Flaker's analog circuit. Accordingly, we cannot sustain the obviousness rejection of claims 7 and 8.

ORDER

The decision of the Examiner rejecting claims 10 through 13 and 15 under 35 U.S.C. § 112, first paragraph, and claims 10 through 13 and 15 through 19 under 35 U.S.C. § 102(a) is affirmed. The decision of the Examiner rejecting claims 6 and 9 under 35 U.S.C. § 102(a) and claims 7 and 8 under 35 U.S.C. § 103 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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